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10/652,134

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Philip E. May

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LEVEQUE INTELLECTUAL PROPERTY LAW, P.C.  
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EXAMINER

PAN, DANIEL H

ART UNIT

PAPER NUMBER

2183

DATE MAILED: 11/22/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

Application No.

10/652,134

Applicant(s)

MAY ET AL.

Examiner

Daniel Pan

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 25 September 2006.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 6,7 and 10-15 is/are pending in the application.
- 4a) Of the above claim(s) 1-5,8 and 9 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 6,7 and 10-15 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 03 May 2006 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO/SB/08)  
Paper No(s)/Mail Date 06/01/06, 05/03/06, 08/29/03.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: \_\_\_\_\_.

1. Claims 6,7, 10-15 are presented for examination. Claims 1-5, 8,9 have been canceled.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

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(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 6,10,11,12 are rejected under 35 U.S.C. 102(b) as being anticipated by Tanaka (5,893,143).

3. As to claim 6, Tanaka also taught :

a) fetching an identifier (see the mask 1100 in 720 in fig.6) having one bit for each element of processor (see each control fields in fig.6 [720] [NOP] and [FIELD3-b], see also reinserting of NOP into instruction in col.6, lines 1-2, see also the decompression when the instruction was readout in col.3, lines 6-13), wherein a bit [1] of their identifier was set if a corresponding ordered field contain a NOP instruction (see field [NOP]) in very control word (see the fourth entry of the cache in 720 in fig.6) of a sequence of control words (see entries 1-5 in fig.6 720 for a sequence of control words, see also col.8, lines 6-56 for how the instruction words being fed to the corresponding processing

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units) for each control word of the compressed sequence of multiple-instruction control words;

b) disabling an element of the processor (see NOP for indicating no operational instruction), to reduce the power consumption if corresponding bit of identifier was set (not explicitly shown), and the element was disabled (no operational);

d) fetching a control word (see read out of instruction in col.10, lines 18-26);

e) executing the control word (see the decompressed instruction for executing in col.8, lines 18-26).

4. As to claim 10, Tanaka taught :

a) a mask latch for storing a compression mask (see mask) that identifies a set of aligned fields removed during compression of the sequence of multiple-instruction control words (see fig.6) ;

b) having one bit for each element of processor (see each control fields in fig.6 [720] [NOP] and [FIELD3-b]), wherein a bit [1] of their identifier was set if a corresponding ordered field contains a NOP instruction (see field [NOP]) in very control word (see the fourth entry of the cache in 720 in fig.6) of a sequence of control words (see entries 1-5 in fig.6 720 for a sequence of control words, see also col.8, lines 6-56 for how the instruction words being fed to the corresponding processing units) for each control word of the compressed sequence of multiple-instruction control words;

c) a logic unit coupled to the mask latch and responsive to the compression mask (see the logic circuit coupled to mask in fig.9 and fig.11);

d) a memory for storing one or more compressed multiple-instruction control

words (see [cache 720 ] in fig.6, and fig.9 and fig.11 memory for storing the mask) ;

e) a pipelined permute unit, coupled to the logic unit and the memory and operable to reconstruct multiple-instruction control words by fetching a compressed multiple-instruction control word from the memory and inserting NOP instructions in accordance with the compression mask (see reinserting of NOP into instruction in col.6, lines 1-2, see also the decompression when the instruction was readout in col.3, lines 6-13) ; and

f) an instruction register coupled the pipelined permute unit and operable to present reconstructed multiple-instruction control words to the processor (see each entry in fig.6).

5. As to claim 11, Tanaka showed a write enabling signal for each memory caches (memory banks). Therefore, Tanaka was able to disable the memory banks. The memory banks remained disabled while the sequence of control words was processed (see the processing of control words and the mask as the identifier in fig.11 for selecting the clusters).

6. As to claim 12 , see the mask as the identifier in fig.11 for selecting the clusters.

7. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka (5,893,143) in view of Pechanek et al. (6,173,389) .

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8. As to claim 13, limitations of parent claim discussed above will not be repeated herein. Tanaka did not specifically show his system was used for vector processing as claimed. However, Pechanek disclosed a system for including a nop operation with a vector processing (e.g. see the background in col.1, lines 35-42). It would have been obvious to one of ordinary skill in the art to use Pechanek in Tanaka for including the vector processing as claimed because the use of Pechanek could provide Tanaka the capability to adapt to different type of processing methods, such as vector processing, and it could be done by configuring the vector of Pechanek with a modified parameters (e.g. the vector registers) into Tanaka, so that the vector processing of Pechanek could be recognized by Tanaka, and since no specific type of vector processing is being recited in the claim, one of ordinary skill in the art should be able to recognize the use of vector processing in general into Tanaka for achieving the fast processing capacity as desired by Tanaka (see Tanaka col.3, lines 37-41).

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

9. Claim 7,14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka (5,893,143) in view of Shebanow et al. (5,367,494).

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10. As to claim 7, 14, limitations of claim 7 were already discussed in paragraphs 3,4 above, therefore, it will not be repeated herein. Tanaka also taught at least :

a) a mask latch for storing a bit mask having one bit for each data path element (see each entry field in fig.6 [720]), wherein a bit of the bit mask is set [1] if a corresponding ordered field contains a NOP instruction (see NOP field) in every multiple-instruction control word [each entry] of the sequence of control words (see entries of fig.6 [720] for the sequence of control words);

b) a plurality of memory banks operable to store instructions of a multiple- instruction control word (see fig.6 cache);

c) a plurality of data path elements (see the fields in a given entry);

d) a logic unit coupled to the mask latch, and

e) an instruction register, coupled to the memory banks and operable to present instructions the datapath elements (see each entry in fig.6).

11. Tanaka did not specifically show that his write signal was used for enabling and disabling of the subset of memory banks as claimed. However, Shebanow taught a system for enabling a subset of memory banks (see Abstract , see also the enabling of memory banks on the control value A and B in col.11, lines 5-68, col.12, lines 1-27). It would have been obvious to one of ordinary skill in the art to sue Shebanow in Tanaka for enabling/disabling the subset of memory banks as claimed because the use of Shebanow could provide Tanaka the ability to accept and send data from a plurality of memory sets at a given cycle, therefore, increasing the bandwidth of the storage access control , and because Tanaka also taught to provide



a plurality of processing units with corresponding memory caches (the banks) for execution in parallel (see col.3, lines 52-63), and also showed a write enabling signal for each memory caches (see the processing of control words and the mask as the identifier in fig.11 for selecting the clusters), which was a suggestion of the need for disabling a memory of plurality of memory banks in order to provide data to the plurality of processing units in parallel, and for doing so, provide a motivation.

12. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka (5,893,143) in view of Shebanow et al. (5,367,494), as applied to claim 14, and further in view of Pechanek et al. (6,173,389).

13. Neither Tanaka nor Shebanow specifically show the vector processor as claimed. However, Pechanek disclosed a system for including a nop operation with a vector processing (e.g. see the background in col.1, lines 35-42). It would have been obvious to one of ordinary skill in the art to use Pechanek in Tanaka for including the vector processing as claimed because the use of Pechanek could provide Tanaka the ability to accept different type of processing (e.g. the vector processing, or the like) and it could be achieved by defining the vector register of Pechanek with a modified width or control variable into the configuration file of Tanaka, therefore the vector registers of Pechanek could be recognized by Tanaka, and since no specific type of vector processing is being recited in the claim, one of ordinary skill in the art should be able to recognize the use of vector processing in general into Tanaka for achieving the fast processing capacity as desired by Tanaka (see Tanaka col.3, lines 37-41), in doing so, provided a motivation.



14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a) Mehrotra et al. (6,571,016) is cited for a system including a loop (routine) for computation in a personal computer (e.g. see the decompressing routine used by personal computer in col.7, lines 46-55);

b) Lowe, Jr. (5,542,084) is cited for the background teaching of the mask disabling the memory banks or sections (see col.1, lines 42-47).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Pan whose telephone number is 571 272 4172.

The examiner can normally be reached on M-F from 8:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan, can be reached on 571 272 4162. The fax phone number for the organization where this application or proceeding is assigned is 703 306 5404.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should

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you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

## ***21 Century Strategic Plan***

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